with a control gate voltage V_{SH} in step 901 followed by a second read with a control gate voltage V_{SL} in step 904. The values of these voltage levels are shown in Figure 10, where the states with poor data retention will correspond to the region above V_{SL} and below V_{SH}. An incorrect reading in step 901 results from a threshold voltage, corresponding to stored charge level, being below the second reference level, while an incorrect reading in step 903 results from a threshold voltage being above the second reference level. Thus, this describes the process of identifying a second sector with one or more cells having a threshold level above the first reference level and below the second reference level, or, since the threshold level is dependent upon a cell's charge level, as described in the application (for example, beginning on page 2 at line 17) and is basic to the operation of a charge storing non-volatile memory, the process describes "identifying a second sector of said memory cells having one or more memory cells with a charge above the first reference level and below the second reference level".

Consequently, the rejection of claim 46, along with dependent claims 47-50, under 35 U.S.C. 112, first paragraph, is respectfully submitted to be without foundation.

Claim 42

The Office Action also states that it fails to find support for the second element of claim 42, "identifying a memory cell of the set having a charge above the first reference level and below the second reference level". It is respectfully submitted that this element is fully supported by the specification. This is similar in scope to the limitation discussed with respect to claim 46 above, except that instead of identifying a second sector having one or more memory cells in a degraded state, the method identifies a degraded memory cell in the set of previously written cells. Therefore, claim 42 is supported by the same portion of the disclosure as described with respect to claim 46, except for the embodiment where the identification is performed for the same set of cells instead of those in a different sector.

Consequently, the rejection of claim 42, along with dependent claims 43-45, under 35 U.S.C. 112, first paragraph, is respectfully submitted to be without foundation.

Claims 37 and 39

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The Office Action also rejected independent claims 37 and 39 under 35 U.S.C. 112, first paragraph. In particular, the Office Action fails to find support in the present application for the process of "programming the memory cell until the charge of the memory cell is above the programmed-cell reference level", found in claim 37, and "programming each memory cell of the group of one or more cells until each of the memory cells has a stored charge over the second threshold", found in claim 39.

On page 4, lines 15-17, the Office Action does state that "[i]n Figure 8, a check is performed to see if all cells are correctly written under the control of an applied voltage, and if the data are read correctly, a program verify operation is considered to have been successfully [sic]." That is, the Office Action does admit that application does describe a program verify-operation in which the memory cells are determined to be properly programmed. As described in the application at page 23, lines 27-30, this is accomplished by reading the cells with a control gate set to the program verify level V_{PV} shown in Figure 10.

The read value of a floating gate memory cell at a reference voltage during the verify process is indicative of the threshold voltage of the cell, which is turn determined by the stored charge of the memory cell. This is standard in the operation of charge storing non-volatile memory cells and is described more fully in the application beginning on page 2, line 17:

> Essentially, EEPROM or Flash EEPROM are field effect transistors each with an additional polysilicon region generally referred to as the floating gate. Data is "memorized" through confinement of predefined amounts of electric charge in this floating gate.
>
> The electric charge are transferred to the floating gate from the substrate through a dielectric region. They effect the conductivity of the source-drain channel and the threshold voltage of the field effect transistor. Physically, the differences in threshold voltages and the differences in source-drain currents, due to the confinement of different amounts of electric charge in the floating gates, can then be used to define different logic states (e.g. "0", "1", ...). Demarcation threshold voltage levels may be used to demarcate between the different logic states. For example, a "0" or "1" state would respectively have a programmed threshold voltage level less than or greater than the demarcation threshold between these two states.

Thus, the Office Action admits that the present application has support for programming the identified memory cells until they verify at the programmed cell level, and, as the preceding quote make clear, this programmed cell level is indicative of the charge of the memory cell being above the programmed-cell reference level. Consequently, the present

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application has support for "programming the memory cell until the charge of the memory cell is above the programmed-cell reference level" and "programming each memory cell of the group of one or more cells until each of the memory cells has a stored charge over the second threshold".

For these reasons, the rejection of claims 37 and 39, along with dependent claims 40 and 41 under 35 U.S.C. 112, first paragraph, is respectfully submitted to be without foundation.

Conclusion

Therefore, it is respectfully submitted that the present application fully supports the claimed subject matter and that a rejection under 35 U.S.C. 112, first paragraph, is not well founded, and that claims 37 and 39-50 are allowable. Reconsideration of the Office Action's rejection of claims 37 and 39-50, and a prompt declaration of the previously requested interference is respectfully requested.

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Respectfully submitted,

MGC

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1-30-2003
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